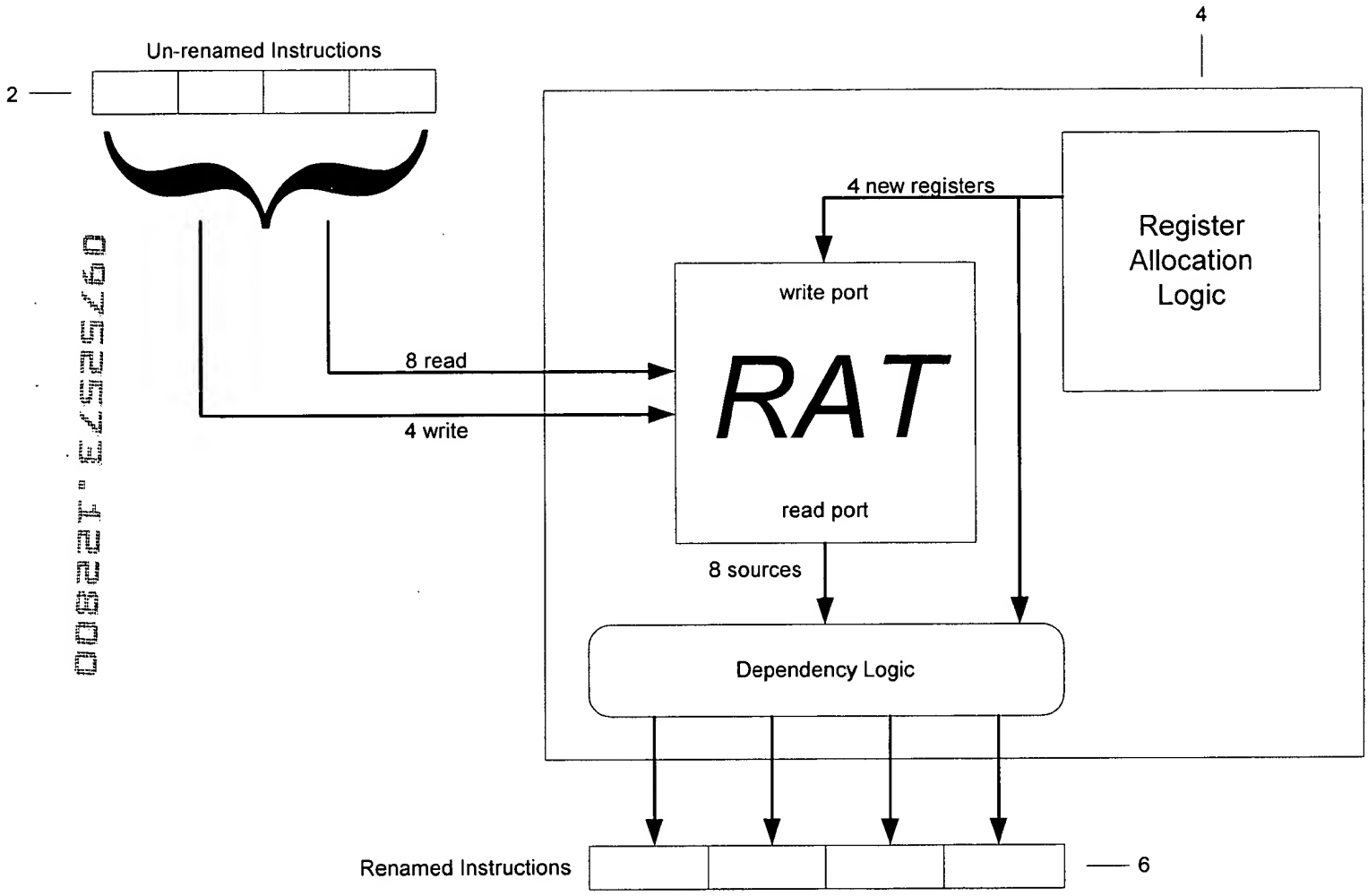
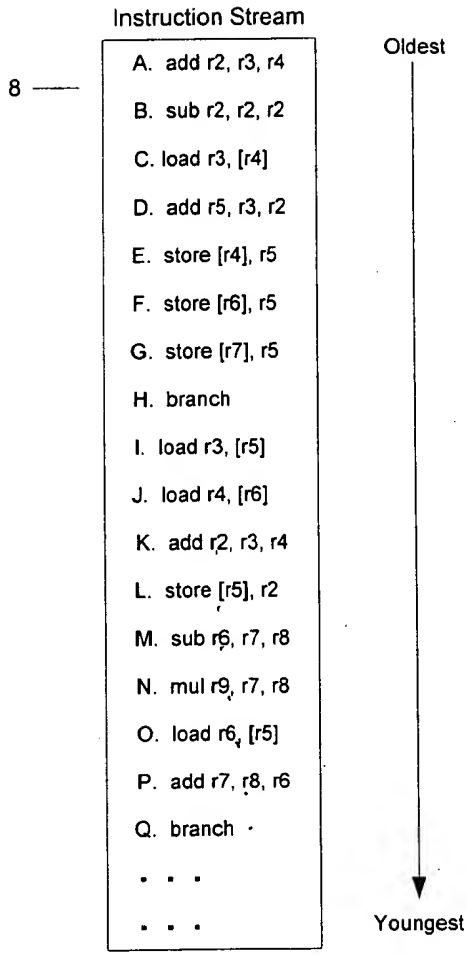

4
Un-renamed Instructions
2
4 new registers
Register Allocation Logic
write port
RAT
read port
8 read
4 write
8 sources
Dependency Logic
Renamed Instructions
6

Figure 1


Instruction Stream
8
A. add r2, r3, r4
B. sub r2, r2, r2
C. load r3, [r4]
D. add r5, r3, r2
E. store [r4], r5
F. store [r6], r5
G. store [r7], r5
H. branch
I. load r3, [r5]
J. load r4, [r6]
K. add r2, r3, r4
L. store [r5], r2
M. sub r6, r7, r8
N. mul r9, r7, r8
O. load r6, [r5]
P. add r7, r8, r6
Q. branch
Oldest
Youngest

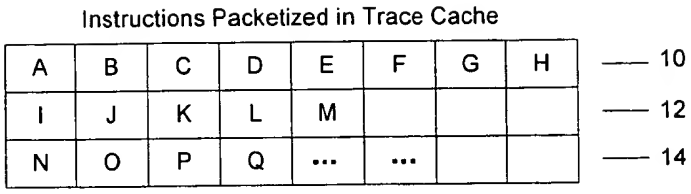

Instructions Packetized in Trace Cache
A B C D E F G H
I J K L M
N O P Q ... ...
10
12
14

Figure 2

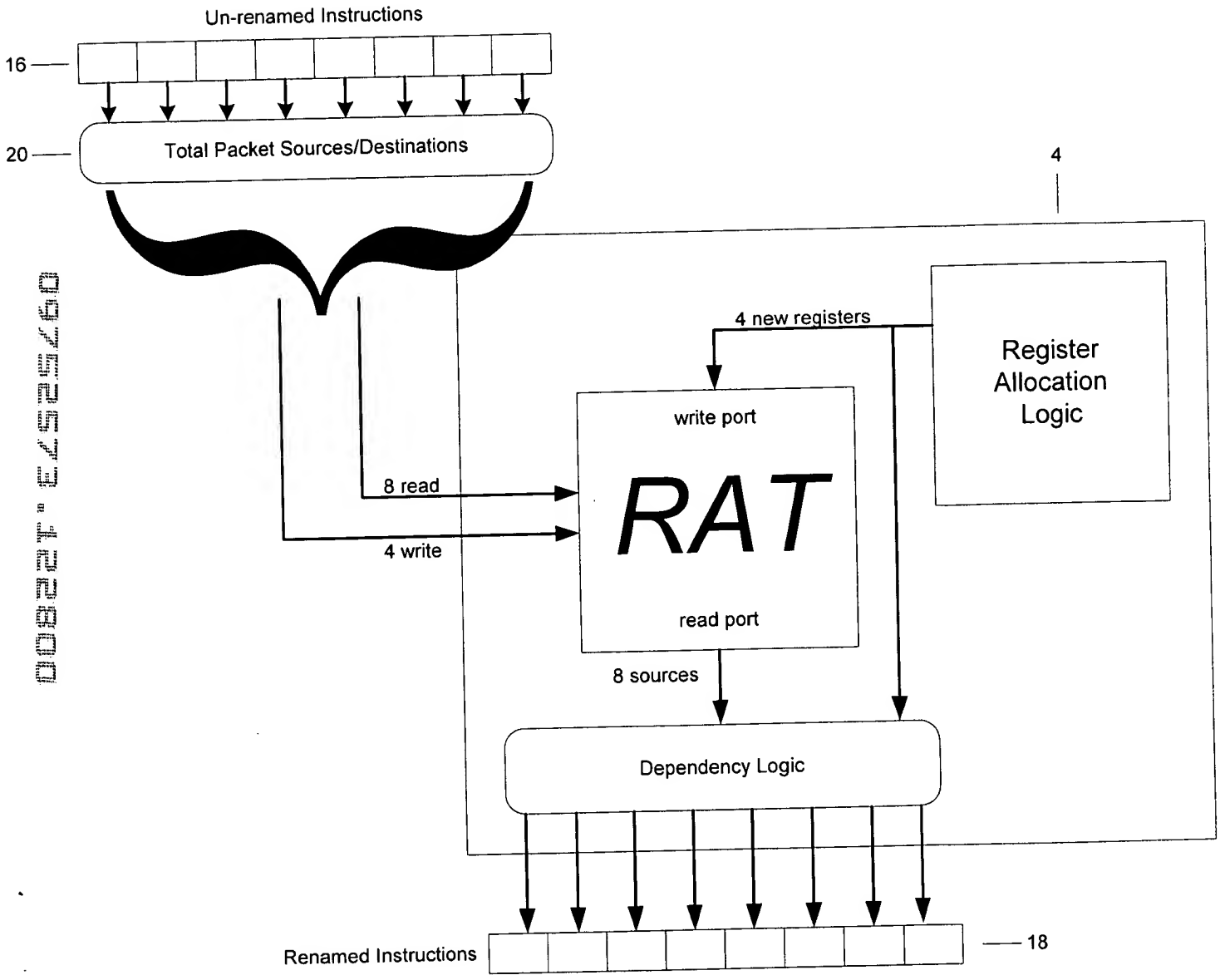

Un-renamed Instructions
16
20
Total Packet Sources/Destinations
4
4 new registers
Register Allocation Logic
write port
RAT
read port
8 read
4 write
8 sources
Dependency Logic
Renamed Instructions
18

Figure 3